#16 04-22-04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	**09/471,200**
Applicant	:	**Bachrach, Y.**
Filed	:	**12/23/1999**
TC/AU	:	**2112**
Examiner	:	**Vo, Tim T.**
Docket No.	:	**p7291**

Confirmation No. **7140**

I hereby certify that this correspondence is being deposited with the United Service as first class mail with sufficient postage in an envelope addressed t Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450

on April 19, 2004
Date of Deposit

Anne Collette
Name of Person Mailing Correspondence

Anne Collette 4/19/2004
Signature Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

04/22/2004 DHALL1 00000002 022666 09471200

03 FC:1402 330.00 DA

Appeal Brief under 37 C.F.R. §1.192

Assistant Commissioner for Patents:

The applicant ("Applicant") respectfully submits this Brief in triplicate in support of his appeal from a final decision by the Examiner in the above-identified case.

An oral hearing is not desired.

1. Real Party of Interest

Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052, is the assignee of the present invention and the real party of interest.

2. Related Appeals and Interferences

To the best of Applicants' knowledge, there are no appeals or interferences related to the present Appeal which will directly affect, be directly affected by, or have a bearing on the Board's decision.

3. Status of the Claims

Claims 1, 3, 5, 7, and 9-15 are presently active.

Claims 1, 3, 5, 7, and 9-15 stand rejected under 35 U.S.C. §102(b), as being anticipated by Runaldue, et al., US patent 6,108,726 ("Runaldue").

4. Status of Amendments

No amendment has been filed subsequent to the final rejection.

5. Summary of the Invention

The present invention is directed to a network interface device. More particularly, the present invention is directed to a PHY (Physical Layer) and MAC (Media Access Control Layer). The PHY and MAC layers communicate with each other in which communication between the PHY and the MAC is in the form of PHY-to-MAC words and MAC-to-PHY words. A PHY-to-MAC word is a word that is sent by the PHY to the MAC, and a MAC-to-PHY word is a word that is sent by the MAC to the PHY. Each PHY-to-MAC word is pair synchronized with a MAC-to-PHY word. That is, a PHY-to-MAC word is sent by the PHY to the MAC synchronously with a MAC-to-PHY word sent by the MAC to the PHY. (See, for example, page 4, lines 22-28, of the present application.)

A word may contain data or control information. By providing a communication interface between the PHY and the MAC such that pair-wise synchronized words are communicated, a flexible communication interface is realized, allowing for a MAC to communicate with more than one type of PHY. In addition, the PHY comprises a register to store a pointer to memory, so that the computer system may load the proper device driver independently of the BIOS being loaded.

6. Issue

Whether claims 1, 3, 5, 7, and 9-15 are anticipated by Runaldue.

7. Grouping of Claims

Applicants assert that all of the claims at issue fall into one group.

All of the claims recite the limitation of ports for transmitting and/or receiving PHY-to-MAC words and MAC-to-PHY words that are synchronized into pairs. For this

reason, Applicant believes that for purposes of this Appeal, the claims may be grouped into one group.

8. Argument

In the final office action mailed 18 December 2003 ("Office Action"), page 2, it was indicated that Runaldue teaches a PHY to provide data to a MAC via PHY-to-MAC words and to receive data and commands from the MAC via MAC-to-PHY words. Furthermore, it was indicated on page 3 of the Office Action that these words are synchronized into pairs, where reference was made to Figs. 2-3 and column 3, line 35 to column 4, line 19, of Runaldue. Applicant respectfully traverses these statements in the Office Action.

Nowhere does Runaldue teach an interface between a PHY and a MAC that is both word based and synchronized so that these words are sent in pairs. The interface depicted in Runaldue (see Figs. 3 and 4) shows a communication interface between a MAC and a PHY that utilizes multiplexing to reduce pin count. But nowhere does Runaldue teach that this communication is via pair-synchronized words.

For example, referring to Fig. 3 of Runaldue, there is a CLOCK signal line, a TXDATA signal line, and a RXDATA signal line. As discussed in Runaldue, column 3, starting at near line 40, TXDATA is multiplexed output from the MAC to the PHY and consists of data to be transmitted onto the network, and RXDATA is multiplexed input from the PHY to the MAC is data received from the network. Both TXDATA and RXDATA are synchronous with CLOCK. However, because TXDATA is data to be transmitted onto the network and RXDATA is received data, TXDATA is not sent by the MAC to the PHY at the same time that RXDATA is sent from the PHY to the MAC. That is, they are not synchronized into pairs. So, even if these were to be identified as "1-bit" words, they are not pair synchronized.

Applicant respectfully asserts that the Office Action does not point out where in Runaldue it is taught that pair-synchronized words are transferred between the PHY and the MAC.

Conclusion

For the above reasons, the Board is respectfully requested to vacate the Examiner's rejection of the pending claims, to remand this application to the Examiner, and to direct the Examiner to pass this case to issuance.

Respectfully submitted,

Seth Z Kalson Dated: 4-15-04

Seth Z. Kalson
Reg. no. 40,670
Attorney for Applicants and Intel Corporation (Assignee)

9. Appendix

1. (Previously Presented) A PHY (Physical Layer) to provide data to a MAC (Media Access Control) via PHY-to-MAC words and to receive data and commands from the MAC via MAC-to-PHY words, the PHY comprising:

at least one PHY-to-MAC port to provide signals indicative of the PHY-to-MAC words;

at least one MAC-to-PHY port to receive signals indicative of the MAC-to-PHY words;

a register to store a pointer to a memory location so as to provide identification information about the PHY; and

at least one Reset/Sync port to receive a signal to provide synchronization so that the PHY-to-MAC words and MAC-to-PHY words are synchronized into pairs, wherein a pair comprises one MAC-to-PHY word and one PHY-to-MAC word.

2. (Cancelled)

3. (Previously Presented) A MAC (Media Access Control) to provide data and commands to a PHY (Physical layer) via MAC-to-PHY words and to receive data from the PHY via PHY-to-MAC words, the MAC comprising:

at least one MAC-to-PHY port to provide signals indicative of the MAC-to-PHY words;

at least one PHY-to-MAC port to receive signals indicative of the PHY-to-MAC words; wherein the at least one PHY-to-MAC port receives a signal indicative of a

pointer to a memory location so as to provide identification information about the PHY; and

at least one Reset/Sync port to provide a signal to synchronize the PHY-to-MAC words and MAC-to-PHY words into pairs, wherein a pair comprises one MAC-to-PHY word and one PHY-to-MAC word.

4. (Cancelled)

5. (Previously Presented) A chipset comprising:

a MAC (Media Access Control) to provide data and commands to a PHY (Physical layer) via MAC-to-PHY words and to receive data from the PHY via PHY-to-MAC words, wherein the MAC comprises:

at least one MAC-to-PHY port to provide signals indicative of the MAC-to-PHY words;

at least one PHY-to-MAC port to receive signals indicative of the PHY-to-MAC words; wherein the at least one PHY-to-MAC port receives a signal indicative of a pointer to a memory location so as to provide identification information about the PHY; and

at least one Reset/Sync port to provide a signal to synchronize the PHY-to-MAC words and MAC-to-PHY words into pairs, wherein a pair comprises one MAC-to-PHY word and one PHY-to-MAC word.

6. (Cancelled)

7. (Original) The chipset as set forth in claim 5 further comprising a register, wherein the chipset loads the identification information into the register.

8. (Cancelled)

9. (Previously Presented) A computer system comprising:

a first memory device;

a MAC (Media Access Control);

a PHY (Physical layer) to provide data to the MAC via PHY-to-MAC words and to receive data and commands from the MAC via MAC-to-PHY words, the PHY comprising:

at least one PHY-to-MAC port to provide signals indicative of the PHY-to-MAC words;

at least one MAC-to-PHY port to receive signals indicative of the MAC-to-PHY words; and

a register to store a pointer to a memory location in the first memory device so as to provide identification information about the PHY;

wherein the PHY-to-MAC words and the MAC-to-PHY words are synchronized into pairs, where a pair comprises one PHY-to-MAC word and one MAC-to-PHY word.

10. (Original) The computer system as set forth in claim 9, wherein the MAC further comprises a register to store the identification information.

11. (Original) The computer system as set forth in claim 9, further comprising:

a processor;

system memory;

secondary memory to store a device driver for the PHY; wherein the processor loads the device driver from the secondary memory into system memory based upon the identification information.

12. (Original) The computer system as set forth in claim 11, wherein the MAC further comprises a register to store the identification information.

13. (Previously Presented) The computer system as set forth in claim 11, further comprising a second memory device to store BIOS (Basic Input Output System), wherein the processor loads the device driver independently of loading the BIOS.

14. The computer system as set forth in claim 12, further comprising a second memory device to store BIOS, wherein the processor loads the device driver independently of loading the BIOS.

15. (Original) The computer system as set forth in claim 14, further comprising:

a system bus; and

a chipset in communication with the system bus, wherein the MAC is integrated with the chipset.